The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-60. (Canceled)

61. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a resin black matrix over a second substrate;

forming a second organic leveling film over said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

62. (Previously Presented) A method according to claim 61 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

63. (Previously Presented) A method according to claim 61 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

64. (Previously Presented) A method according to claim 61 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

65. (Previously Presented) A method according to claim 61 wherein said gate electrode comprises aluminum.

66. (Previously Presented) A method according to claim 61 wherein said gate insulating film comprises silicon oxide.

67. (Previously Presented) A method according to claim 61 wherein said amorphous semiconductor film is deposited through plasma CVD.

68. (Previously Presented) A method according to claim 61 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

69. (Previously Presented) A method according to claim 61 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

70. (Previously Presented) A method according to claim 61 wherein said pixel electrode extends over said channel region.

71. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a resin black matrix over said second substrate;

forming a second organic leveling film over said color filter and said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

72. (Previously Presented) A method according to claim 71 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

73. (Previously Presented) A method according to claim 71 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

74. (Previously Presented) A method according to claim 71 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

75. (Previously Presented) A method according to claim 71 wherein said gate electrode comprises aluminum.

76. (Previously Presented) A method according to claim 71 wherein said gate insulating film comprises silicon oxide.

77. (Previously Presented) A method according to claim 71 wherein said amorphous semiconductor film is deposited through plasma CVD.

78. (Previously Presented) A method according to claim 71 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

79. (Previously Presented) A method according to claim 71 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

80. (Previously Presented) A method according to claim 71 wherein said pixel electrode extends over said channel region.

81.-90. (Canceled)

91. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a resin black matrix over a second substrate;

forming a second organic leveling film over said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

92. (Previously Presented) A method according to claim 91 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

93. (Previously Presented) A method according to claim 91 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

94. (Previously Presented) A method according to claim 91 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

95. (Previously Presented) A method according to claim 91 wherein said gate electrode comprises aluminum.

96. (Previously Presented) A method according to claim 91 wherein said gate insulating film comprises silicon oxide.

97. (Previously Presented) A method according to claim 91 wherein said amorphous semiconductor film is deposited through plasma CVD.

98. (Previously Presented) A method according to claim 91 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

99. (Previously Presented) A method according to claim 91 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

100. (Previously Presented) A method according to claim 91 wherein said pixel electrode extends over said channel region.

101. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a resin black matrix over said second substrate;

forming a second organic leveling film over said color filter and said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

102. (Previously Presented) A method according to claim 101 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

103. (Previously Presented) A method according to claim 101 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

104. (Previously Presented) A method according to claim 101 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

105. (Previously Presented) A method according to claim 101 wherein said gate electrode comprises aluminum.

106. (Previously Presented) A method according to claim 101 wherein said gate insulating film comprises silicon oxide.

107. (Previously Presented) A method according to claim 101 wherein said amorphous semiconductor film is deposited through plasma CVD.

108. (Previously Presented) A method according to claim 101 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

109. (Previously Presented) A method according to claim 101 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

110. (Previously Presented) A method according to claim 101 wherein said pixel electrode extends over said channel region.

111.-128. (Canceled)